



Preliminary Data Sheet

S10430

AMI Microsystems GmbH  
 ROSENHEIMER STR. 30/32 SUITE 237  
 8000 MUNICH 80, GERMANY  
 TEL(09) 48-30-81

DIVIDER-KEYER

Features

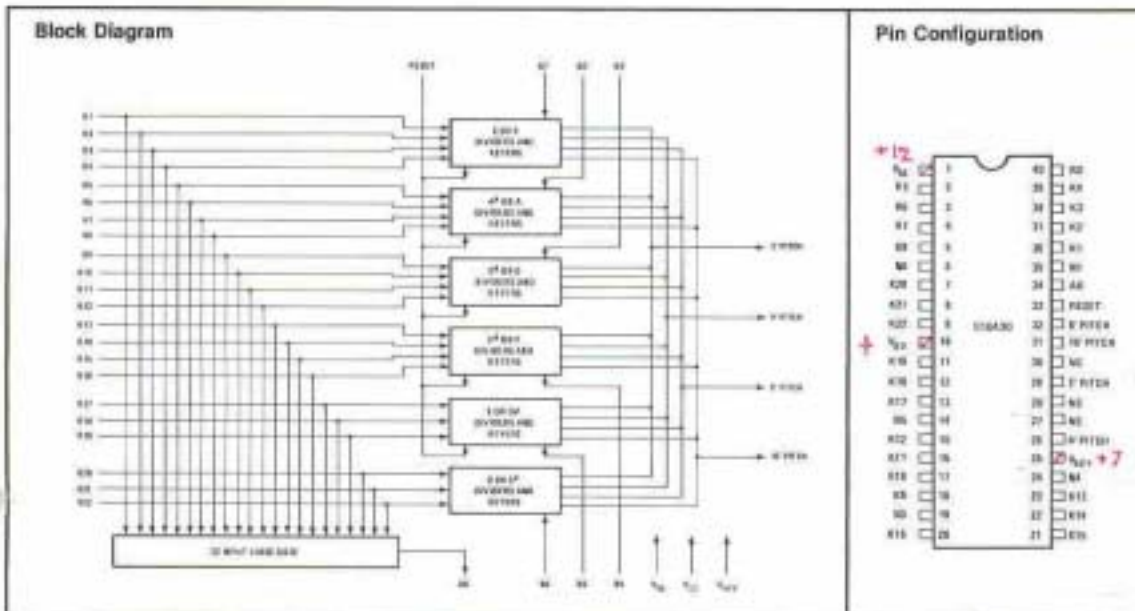
- 22 Keyboard Inputs
- 88 DC Keyer Circuits
- 34 Binary Dividers
- Provides Four Pitch Outputs
- All Key Inputs Sustainable for Percussion
- All Dividers Resettable
- Provides "Any Key Down" Indication
- Eliminates Multiple-Contact Key Switches

Typical Applications

- Generation and Keying of Musical Tones
- Standard Spinet Organ Keying (37 or 44 note keyboards)
- Keying of Sustained Tones
- Percussive Effects
- Generating Stair-stepped Waveforms
- Electronic Piano

General Description

The S10430 divider-keyer is a monolithic integrated circuit fabricated with P-Channel Ion-implanted MOS technology. It is intended for use in spinet organs or other electronic musical instruments having keyboards of up to 44 keys. This device has 22 key inputs, allowing all keying functions for a 44 note manual to be performed by two S10430 circuits. Each S10430 accepts six frequencies from a top octave synthesizer, such as an S50240, and provides squarewave outputs at 16 foot, 8 foot, 4 foot, and 2 foot pitches. For example, if a C key is depressed by itself a low C frequency appears at the 16 foot output, and a C frequency one octave higher appears at the 8 foot output; similarly, the 4 foot and 2 foot outputs provide C frequencies one and two octaves higher, respectively, than the C frequency of the 8 foot output. All appropriate frequency division is performed by the S10430, eliminating the need for external dividers.



**General Description (Continued)**

The circuit also eliminates the need for multiple-contact key switches and discrete diode or transistor keyers. Because of the high input impedance of the

MOS keyers used in this circuit, long sustain envelopes may be obtained by connecting low-value capacitors to the keying inputs.

**Absolute Maximum Ratings**

Voltage on Any Pin Relative to $V_{SS}$	+0.3V to -27.0V
Operating Temperature (ambient)	0°C to 70°C
Storage Temperature	-65°C to 150°C

**Electrical Characteristics**

0°C <  $T_A$  < 70°C;  $V_{SS} = 0V$ ;  $V_{DD} = -12.6V$  to  $-15.4V$ ;  $V_{KEY} = -4.75V$  to  $-5.25V$  (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_L$	Logic Low Level TOS and Reset Inputs	0.0		0.8	V	
$V_{HS}$	Logic High Level TOS and Reset Inputs	-4.2		$V_{DD}$	V	
$t_r, t_f$	Rise and Fall Times TOS Inputs			50	$\mu\text{sec}$	Measured between 10% and 90% points
$V_{OL}$	Logic Low Level AK Output		-0.5	-1.0	V	100K $\Omega$ load to $V_{DD}$
$t_{10}$	Transition of AK Output to 10% of $V_{DD}$			10	$\mu\text{s}$	100pF and 100K $\Omega$ load to $V_{DD}$
$F_T$	Operating Frequency TOS Inputs	DC		50K	Hz	
$D_D$	Output Duty Factor	48		52	%	Measured between 10% and 90% points
$I_{KA}$	Peak Output Current Absolute (any pitch output with 1 keyer on)	350		650	$\mu\text{A}$	$V_{DD} = -14V$ $V_{KEY} = -5V$ $V_{EN} = -26V$ <i>+12V -12</i> $T_A = 25^\circ\text{C}$
$I_p$	Peak Output Current	85		115	% $I_{AVE}$	$V_{DD} = -14V$ $V_{KEY} = -5V$ $V_{EN} = -25V$ $T_A = 25^\circ\text{C}$
$I_p$	Peak Output Current	50		75	% $I_{AVE}$	$V_{DD} = -14V$ $V_{KEY} = -5V$ $V_{EN} = -15V$ $T_A = 25^\circ\text{C}$
$I_p$	Peak Output Current	0.5			$\mu\text{A}$	$V_{DD} = -14V$ $V_{KEY} = -5V$ $V_{EN} = -3.0V$ $T_A = 25^\circ\text{C}$
$I_p$	Peak Output Current			0.5	$\mu\text{A}$	$V_{DD} = -14V$ $V_{KEY} = -5V$ $V_{EN} = -1.0V$ $T_A = 25^\circ\text{C}$

\* $I_{AVE}$  is the average of all peak output current values within one circuit.

### Functional Description

The S10430 Divider-Keyer circuit accepts six frequencies as inputs and uses these to clock six binary divider chains. Four of these chains consist of six binary dividers each and the remaining two have five. The six chains generate all frequencies necessary to obtain 2', 4', 8', and 16' pitches for half of a 44 key keyboard.

The outputs of the divider chains are routed to chopper keyer circuits like the one shown in figure 2. When a negative voltage is applied to any "K" input, four of these keyer circuits are turned on to route the appropriate frequencies to each of the four pitch outputs.

Figure 1:  
Typical Time Constants For Sustain Keying

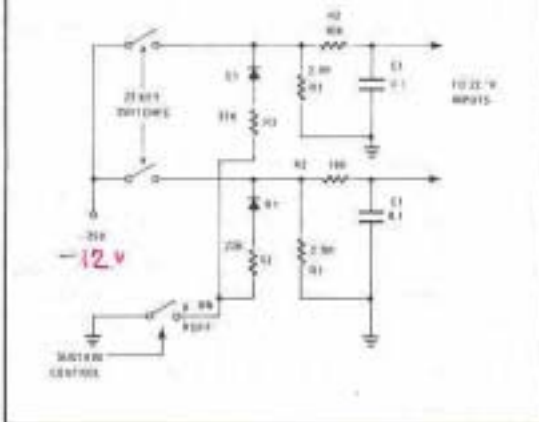
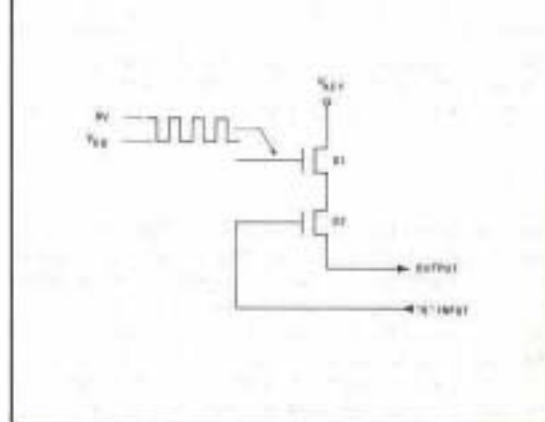


Figure 2:  
Schematic Diagram of Chopper Keyer Circuit



### N Inputs

Six of the twelve tempered scale frequencies are applied to the inputs N1 through N6. Typically, these frequencies would be six of the outputs of a top octave synthesizer, such as an S50240. In general, it doesn't matter which frequencies are applied to the N inputs, although this affects which keyboard keys should be connected to the K inputs. One exception to this arises from the fact that a 44 note keyboard contains more of some keys than others. Specifically, there are only three each of the keys, C#, D, D#, and E, but there

are four each of the keys F, F#, G, G#, A, A#, and C. This results in the requirement that each of the two S10430 divider keyers in a system take two frequencies from the first group, and four from the second group. Stating this another way, the N1, N2, N3, and N4 inputs must have frequencies chosen from the group, F, F#, G, G#, A, A#, B, and C. The N5 and N6 inputs are chosen from the group, C#, D, D#, and E. The example in Figure 4 shows one divider keyer handling the notes, A, A#, B, C, C#, and D while the other does the keying for D#, E, F, F#, G, and G#.

Table 1: Relationship between K and N inputs

INPUT	PIN NO.	OUTPUT (8' PITCH)* PIN 32	INPUT	PIN NO.	OUTPUT (8' PITCH)* PIN 32
K1	36	N1+4	K12	15	N3+32
K2	37	N1+8	K13	23	N4+4
K3	38	N1+16	K14	22	N4+8
K4	39	N1+32	K15	21	N4+16
K5	2	N2+4	K16	20	N4+32
K6	3	N2+8	K17	13	N5+4
K7	4	N2+16	K18	12	N5+8
K8	5	N2+32	K19	11	N5+16
K9	18	N3+4	K20	7	N6+4
K10	17	N3+8	K21	8	N6+8
K11	16	N3+16	K22	9	N6+16

\*To determine outputs for 4' pitch: multiply 8' pitch output by 2.  
 To determine outputs for 2' pitch: multiply 8' pitch output by 4.  
 To determine outputs for 16' pitch: multiply 8' pitch output by

### K Inputs

The twenty-two inputs are connected either directly to key switches or to an attack/decay circuit, such as the one shown in Figure 1. When a negative voltage is applied to any K input, four chopper keyer circuits are turned on, and the appropriate frequencies appear at the four pitch outputs. The amount of current at the output is determined by the voltage at the K input. As the voltage becomes more negative, more current appears at the output. This will be discussed further in the section on "Pitch Outputs."

Connection of the K inputs to the key switches is dependent on which frequencies are applied to which N inputs. Table 1 shows the relationship between the K and N inputs. If, for example, the top octave frequency F, 5588 Hz, is applied to the N2 input, K5 should then be connected to the highest F key on the keyboard, K6 to the next highest, K7 to the next, and K8 to the lowest F. If the highest F key is depressed, then N2+4, or 1397 Hz would appear at the 8' Pitch Output. At the same time, the 16' pitch, 4' pitch and 2' pitch outputs would provide, respectively, 699 Hz, 2794 Hz, and 5588 Hz. An example of K and N input connections is given in Figure 4.

To control attack, decay, and sustain times, a circuit such as the one shown in Figure 1 may be used. When a keyswitch is closed, the K input charges to -25 volts through the time constant of R2 and C1. This

causes the attack time to be about 1ms. If the sustain is on (sustain switch open), when the keyswitch is opened, the K input will charge slowly back to  $V_{SS}$  through the time constant of C1, R1, and R2. This results in a sustain envelope of 271ms. Longer sustains can be obtained with larger capacitors. If the sustain switch is closed, then the decay time is governed by the time constant of C1, R2, and R3 || R1. In this example, this non-sustain decay is about 3ms.

### Pitch Outputs

The outputs labeled 2' pitch, 4' pitch, 8' pitch, and 16' pitch provide the appropriate frequencies for these four pitches depending on which K inputs have been selected. The selected frequencies of the outputs are shown in Table 1. The highest octave of frequencies is obtained directly from the N inputs. Although these top octave frequencies are buffered internally, their duty cycle depends on the duty cycle of the N inputs.

Each output is connected to the outputs of 22 of the chopper keyer circuits shown in Figure 2. The chopper device, D1, is much lower in impedance than the keyer device D2. The output voltage amplitude is dependent, therefore, on the ratio of D2 to the output load. Higher output sink resistor values result in higher output signal amplitudes. However, it is important to keep the output sink resistor low in order to minimize the effects of intermodulation distortion between keyers. Figure 3 shows a typical output waveform with a 100 sink resistor. Because of the need for a low value sink

resistor and the usual desirability of a high signal amplitude, it may be advisable in some cases to load the pitch outputs with operational amplifiers instead of resistors.

#### V<sub>KEY</sub> Input

This supply input is used exclusively for the chopper keyer circuits (Figure 2). It is important that this be a low impedance supply in order to minimize intermodulation distortion between keyer circuits.

The voltage on the supply is kept low relative to V<sub>DD</sub> and the K inputs to insure linear operation of the MOS keying circuits.

#### Reset Input

Applying a V<sub>SS</sub> level to this input causes all binary

dividers to be held in the reset state. A logic 1 applied to Reset causes the dividers to function normally. To prevent possible phase cancellation between upper and lower manual systems, it is suggested that an RC network be connected to this input so that the musical instrument will be locked into proper phase relationships when power is first applied. When in the reset condition, all chopper devices are turned on to facilitate testing.

#### AK Output

Whenever any key input is selected, the AK output is actively pulled to V<sub>SS</sub> to indicate that a key is played. This output is open ended (i.e., no pull-up device is provided), and may be left unconnected if not needed.

Figure 3: Typical Keyer Output

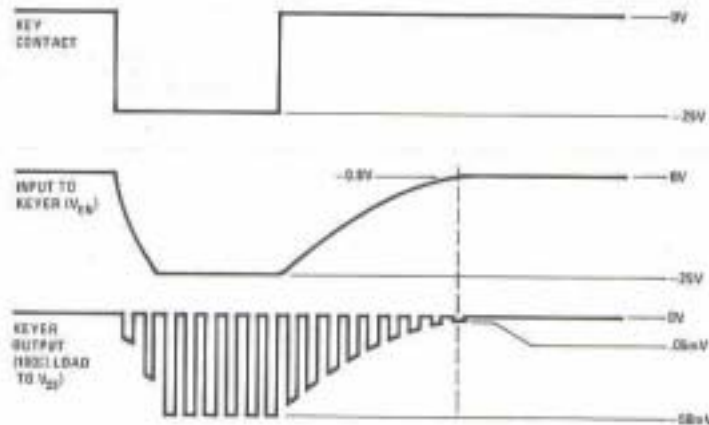


Figure 4: Schematic Diagram of Typical Divider—Keyer Application

